ALGORITHMS FOR SYNTHESIS AND TESTING OF ASYNCHRONOUS CIRCUITS

Edited by

Jonathan Allen



Algorithms For Synthesis And Testing Of Asynchronous Circuits

C. Thomas Gray, Wentai Liu, Ralph K. Cavin, III

Algorithms For Synthesis And Testing Of Asynchronous Circuits:

Algorithms for Synthesis and Testing of Asynchronous Circuits Luciano Lavagno, Alberto L.

Sangiovanni-Vincentelli, 2012-12-06 Since the second half of the 1980s asynchronous circuits have been the subject of a great deal of research following a period of relative oblivion The lack of interest in asynchronous techniques was motivated by the progressive shift towards synchronous design techniques that had much more structure and were much easier to verify and synthesize System design requirements made it impossible to eliminate totally the use of asynchronous circuits Given the objective difficulty encountered by designers the asynchronous components of electronic systems such as interfaces became a serious bottleneck in the design process The use of new models and some theoretical breakthroughs made it possible to develop asynchronous design techniques that were reliable and effective This book describes a variety of mathematical models and of algorithms that form the backbone and the body of a new design methodology for asyn chronous design The book is intended for asynchronous hardware designers for computer aided tool experts and for digital designers interested in ex ploring the possibility of designing asynchronous circuits It requires a solid mathematical background in discrete event systems and algorithms While the book has not been written as a textbook nevertheless it could be used as a reference book in an advanced course in logic synthesis or asynchronous design <u>Logic Synthesis and Verification</u> Soha Hassoun, Tsutomu Sasao, 2012-12-06 Research and development of logic synthesis and verification have matured considerably over the past two decades Many commercial products are available and they have been critical in harnessing advances in fabrication technology to produce today s plethora of electronic components While this maturity is assuring the advances in fabrication continue to seemingly present unwieldy challenges Logic Synthesis and Verification provides a state of the art view of logic synthesis and verification It consists of fifteen chapters each focusing on a distinct aspect Each chapter presents key developments outlines future challenges and lists essential references Two unique features of this book are technical strength and comprehensiveness The book chapters are written by twenty eight recognized leaders in the field and reviewed by equally qualified experts The topics collectively span the field Logic Synthesis and Verification fills a current gap in the existing CAD literature Each chapter contains essential information to study a topic at a great depth and to understand further developments in the field The book is intended for seniors graduate students researchers and developers of related Computer Aided Design CAD tools From the foreword The commercial success of logic synthesis and verification is due in large part to the ideas of many of the authors of this book Their innovative work contributed to design automation tools that permanently changed the course of electronic design by Aart J de Geus Chairman and CEO Synopsys Inc **Application** and Theory of Petri Nets 2000 Mogens Nielsen, Dan Simpson, 2003-06-26 This book constitutes the refereed proceedings of the 21st International Conference on Application and Theory of Petri Nets ICATPN 2000 held in Aarhus Denmark in June 2000 The 20 revised full papers presented together with four invited surveys and four tool presentations were carefully

reviewed and selected from 57 submissions. The papers address all current aspects of Petri net research and development including system design and verification UML compositionality process algebras model checking computer networking business process engineering communication networks etc Various classes of Petri nets are discussed including safe Petri nets high level Petri nets colored Petri nets P T nets and timed Petri nets Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Nadine Azemard, Lars Svensson, 2007-08-21 This volume features the refereed proceedings of the 17th International Workshop on Power and Timing Modeling Optimization and Simulation Papers cover high level design low power design techniques low power analog circuits statistical static timing analysis power modeling and optimization low power routing optimization security and asynchronous design low power applications modeling and optimization and more Electronic Design Automation Frameworks Franz J. Rammig, Flavio Wagner, 2013-04-17 Design frameworks have become an important infrastructure for building complex design systems Electronic Design Automation Frameworks presents a state of the art review of the latest research results covering this topic results which are also of value for other design frameworks The book contains the selected proceedings of the Fourth International Working Conference on Electronic Design Frameworks organized by the International Federation for Information Processing and held in Gramado Brazil in November 1994 Theorem Provers in Circuit Design Ramayya Kumar, Thomas Kropf, 1995-03-06 This two volume set contains papers presented at the International Conference on Computational Engineering Science ICES 95 held in Mauna Lani Hawaii from 30 July to 3 August 1995 The contributions capture the state of the science in computational modeling and simulation in a variety of engineering disciplines civil mechanical aerospace materials and electronics engineering Lectures on Petri Nets II: Applications Wolfgang Reisig, Grzegorz Rozenberg, 1998-11-04 The two volume set originates from the Advanced Course on Petri Nets held in Dagstuhl Germany in September 1996 beyond the lectures given there additional chapters have been commissioned to give a well balanced presentation of the state of the art in the area Together with its companion volume Lectures on Petri Nets I Basic Models this book is the actual reference for the area and addresses professionals students lecturers and researchers who are interested in systems design and would like to learn to use Petri nets familiar with subareas of the theory or its applications and wish to view the whole area interested in learning about recent results presented within a unified framework planning to apply Petri nets in practical situations interested in the relationship of Petri nets to other models of concurrent systems An Analog VLSI System for Stereoscopic Vision Misha Mahowald, 2012-12-06 An Analog VLSI System for Stereoscopic Vision investigates the interaction of the physical medium and the computation in both biological and analog VLSI systems by synthesizing a functional neuromorphic system in silicon In both the synthesis and analysis of the system a point of view from within the system is adopted rather than that of an omniscient designer drawing a blueprint This perspective projects the design and the designer into a living landscape The motivation for a machine centered perspective is

explained in the first chapter The second chapter describes the evolution of the silicon retina The retina accurately encodes visual information over orders of magnitude of ambient illumination using mismatched components that are calibrated as part of the encoding process The visual abstraction created by the retina is suitable for transmission through a limited bandwidth channel The third chapter introduces a general method for interchip communication the address event representation which is used for transmission of retinal data. The address event representation takes advantage of the speed of CMOS relative to biological neurons to preserve the information of biological action potentials using digital circuitry in place of axons The fourth chapter describes a collective circuit that computes stereodisparity In this circuit the processing that corrects for imperfections in the hardware compensates for inherent ambiguity in the environment The fifth chapter demonstrates a primitive working stereovision system An Analog VLSI System for Stereoscopic Vision contributes to both computer engineering and neuroscience at a concrete level Through the construction of a working analog of biological vision subsystems new circuits for building brain style analog computers have been developed Specific neuropysiological and psychophysical results in terms of underlying electronic mechanisms are explained These examples demonstrate the utility of using biological principles for building brain style computers and the significance of building brain style computers for understanding the nervous system Wave Pipelining: Theory and CMOS Implementation C. Thomas Gray, Wentai Liu, Ralph K. Cavin, III, 2012-12-06 The guest for higher performance digital systems for applications such as gen eral purpose computing signal image processing and telecommunications and an increasing cost consciousness have led to a major thrust for high speed VLSI systems implemented in inexpensive and widely available technologies such as CMOS This monograph based on the first author's doctoral dissertation concentrates on the technique of wave pipelining as one method toward achieving this goal The primary focus of this monograph is to provide a coherent pre sentation of the theory of wave pipelined operation of digital circuits and to discuss practical design techniques for the realization of wave pipelined circuits in the CMOS technology Wave pipelining can be applied to a variety of cir cuits for increased performance For example many architectures that support systolic computation lend themselves to wave pipelined realization Also the wave pipeline design methodology emphasizes the role of controlled clock skew in extracting enhanced performance from circuits that are not deeply pipelined Wave pipelining also known as maximal rate pipelining is a timing method ology used in digital systems to increase the number of effective pipeline stages without increasing the number of physical registers in the pipeline Using this technique new data is applied to the inputs of a combinational logic block be fore the outputs due to previous inputs are available thus effectively pipelining the combinational logic and maximizing the utilization of the logic Hardware Design and Petri Nets Alex Yakovlev, Luis Gomes, Luciano Lavagno, 2013-04-17 Hardware Design and Petri Nets presents a summary of the state of the art in the applications of Petri nets to designing digital systems and circuits The area of hardware design has traditionally been a fertile field for research in concurrency and Petri nets Many new ideas about modelling and analysis

of concurrent systems and Petri nets in particular originated in theory of asynchronous digital circuits Similarly the theory and practice of digital circuit design have always recognized Petri nets as a powerful and easy to understand modelling tool. The ever growing demand in the electronic industry for design automation to build various types of computer based systems creates many opportunities for Petri nets to establish their role of a formal backbone in future tools for constructing systems that are increasingly becoming distributed concurrent and asynchronous Petri nets have already proved very effective in supporting algorithms for solving key problems in synthesis of hardware control circuits However since the front end to any realistic design flow in the future is likely to rely on more pragmatic Hardware Description Languages HDLs such as VHDL and Verilog it is crucial that Petri nets are well interfaced to such languages Hardware Design and Petri Nets is divided into five parts which cover aspects of behavioral modelling analysis and verification synthesis from Petri nets and STGs design environments based on high level Petri nets and HDLs and finally performance analysis using Petri nets Hardware Design and Petri Nets serves as an excellent reference source and may be used as a text for advanced courses on the subject

Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits M. Bushnell, Vishwani Agrawal, 2006-04-11 The modern electronic testing has a forty year history Test professionals hold some fairly large conferences and numerous workshops have a journal and there are over one hundred books on testing Still a full course on testing is offered only at a few universities mostly by professors who have a research interest in this area Apparently most professors would not have taken a course on electronic testing when they were students Other than the computer engineering curriculum being too crowded the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook For VLSI the foundation was provided by semiconductor device techn ogy circuit design and electronic testing In a computer engineering curriculum therefore it is necessary that foundations should be taught before applications The field of VLSI has expanded to systems on a chip which include digital memory and mixed signalsubsystems To our knowledge this is the first textbook to cover all three types of electronic circuits We have written this textbook for an undergraduate foundations course on electronic testing Obviously it is too voluminous for a one semester course and a teacher will have to select from the topics We did not restrict such freedom because the selection may depend upon the individual expertise and interests Besides there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course With equal tenacity we address the needs of three other groups of readers

Asymptotic Waveform Evaluation Eli Chiprout, Michel S. Nakhla, 2012-12-06 The intense drive for signal integrity has been at the forefront of and new developments in CAD algorithms Thousands of engineers intent on achieving the best design possible use SPICE on a daily basis for analog simulation and general circuit analysis But the strained demand for high data speeds coupled with miniaturization an unprecedented scale has highlighted the previously negligible effects of interconnects effects which are not always handled appropriately by the present levels of SPICE Signals at these higher

speeds may be degraded by long interconnect lengths compared to the increasingly shorter signal rise times Interconnect structures can be diverse pins connectors leads microstrips striplines etc and present at any of the hierarchical packaging levels integrated circuits printed circuit boards multi chip modules or sys tem backplanes Analysis of these effects in any CAD package has become a necessity Asymptotic waveform evaluation AWE and other moment matching tech niques have recently proven useful in the analysis of interconnect structures and various networks containing large linear structures with nonlinear termi nations Previously all that was available to the designer was a full SPICE simulation or a quick but uncertain timing estimation Moment matching used in linear systems analysis as a method of model reduction describes a method to extract a small set of dominant poles from a large network The information is obtained from the Taylor series coefficients moments of that system Analog Device-Level Layout Automation John M. Cohn, David J. Garrod, Rob A. Rutenbar, Rick Carley, 2012-12-06 This book presents a detailed summary of research on automatic layout of device level analog circuits that was undertaken in the late 1980s and early 1990s at Carnegie Mellon University We focus on the work behind the creation of the tools called KOAN and ANAGRAM II which form part of the core of the CMU ACACIA analog CAD system KOAN is a device placer for custom analog cells ANANGRAM II a detailed area router for these analog cells We strive to present the motivations behind the architecture of these tools including detailed discussion of the subtle technology and circuit concerns that must be addressed in any successful analog or mixed signal layout tool Our approach in organizing the chapters of the book has been to present our algo rithms as a series of responses to these very real and very difficult analog layout problems Finally we present numerous examples of results generated by our algorithms This research was supported in part by the Semiconductor Research Corporation by the National Science Foundation by Harris Semiconductor and by the International Business Machines Corporation Resident Study Program Finally just for the record John Cohn was the designer of the KOAN placer David Garrod was the designer of the ANAGRAM II router and its predeces sor ANAGRAM I This book was architected by all four authors edited by John Cohn and Rob Rutenbar and produced in finished form by John Cohn Timed Boolean Functions William K.C. Lam, Robert K. Brayton, 2012-12-06 Timing research in high performance VLSI systems has advanced at a steady pace over the last few years while tools especially theoretical mechanisms lag behind Much present timing research relies heavily on timing diagrams which although intuitive are inadequate for analysis of large designs with many parameters Further timing diagrams offer only approximations not exact solutions to many timing problems and provide little insight in the cases where temporal properties of a design interact intricately with the design s logical functionalities This book presents a methodology for timing research which facilitates analy sis and design of circuits and systems in a unified temporal and logical domain In the first part we introduce an algebraic representation formalism Timed Boolean Functions TBF s which integrates both logical and timing information of digital circuits and systems into a single formalism We also give a canonical form TBF BDD s for them which can be used for efficient ma nipulation In the second part we apply Timed

Boolean Functions to three problems in timing research for which exact solutions are obtained for the first time 1 computing the exact delays of combinational circuits and the minimum cycle times of finite state machines 2 analysis and synthesis of wavepipelining circuits a high speed architecture for which precise timing relations between signals are essential for correct operations 3 verification of circuit and system performance and coverage of delay faults by testing *Iournal of VLSI Signal* Processing Systems for Signal, Image, and Video Technology, 1998 Asynchronous Circuit Design for VLSI Signal Processing Teresa H. Meng, Sharad Malik, 2011-06-27 Asynchronous Circuit Design for VLSI Signal Processing is a collection of research papers on recent advances in the area of specification design and analysis of asynchronous circuits and systems This interest in designing digital computing systems without a global clock is prompted by the ever growing difficulty in adopting global synchronization as the only efficient means to system timing Asynchronous circuits and systems have long held interest for circuit designers and researchers alike because of the inherent challenge involved in designing these circuits as well as developing design techniques for them The frontier research in this area can be traced back to Huffman s publications The Synthesis of Sequential Switching Circuits in 1954 followed by Unger's book Asynchronous Sequential Switching Circuits in 1969 where a theoretical foundation for handling logic hazards was established In the last few years a growing number of researchers have joined force in unveiling the mystery of designing correct asynchronous circuits and better yet have produced several alternatives in automatic synthesis and verification of such circuits This collection of research papers represents a balanced view of current research efforts in the design synthesis and verification of asynchronous systems Testing and Diagnosis of VLSI and ULSI F. Lombardi, M.G. Sami, 2012-12-06 This volume contains a collection of papers presented at the NATO Advanced Study Institute on Testing and Diagnosis of VLSI and ULSI held at Villa Olmo Como Italy June 22 July 3 1987 High Density technologies such as Very Large Scale Integration VLSI Wafer Scale Integration WSI and the not so far promises of Ultra Large Scale Integration ULSI have exasperated the problema associated with the testing and diagnosis of these devices and systema Traditional techniques are fast becoming obsolete due to unique requirements such as limited controllability and observability increasing execution complexity for test vector generation and high cost of fault simulation to mention just a few New approaches are imperative to achieve the highly sought goal of the three months turn around cycle time for a state of the art computer chip The importance of testing and diagnostic processes is of primary importance if costs must be kept at acceptable levels The objective of this NATO ASI was to present analyze and discuss the various facets of testing and diagnosis with respect to both theory and practice The contents of this volume reflect the diversity of approaches currently available to reduce test and diagnosis time. These approaches are described in a concise yet clear way by renowned experts of the field Their contributions are aimed at a wide readership the uninitiated researcher will find the tutorial chapters very rewarding The expert will be introduced to advanced techniques in a very comprehensive manner **Application and Theory of Petri Nets 1995** Giorgio DeMichelis, Michel Diaz, 1995-06-07 This

book constitutes the proceedings of the 16th International Conference on Application and Theory of Petri Nets held in Torino Italy in June 1995 The 26 revised refereed papers presented were selected from 73 submissions from 22 countries in addition there are abstracts or full papers of the three invited talks All theoretical and applicational aspects are addressed by the contributors coming from industry and academia This volume representatively documents the progress achieved in this application oriented area of research and development since the predecessor conference held one year earlier

Encyclopedia of Microcomputers Allen Kent, James G. Williams, 1997-05-21 Visual Fidelity Designing Multimedia
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