

Choosing RF CMOS or SiGe BiCMOS in mixed-signal design

Deciding what technology to choose for fast-moving targets is not trivial, especially in the commercial space where the price, time to market, and the performance of the chip can make or break a product, and sometimes the company. This article attempts to analyze these issues from the perspective of a fabless design house. It discusses key issues that need to be considered when deciding what technology to choose for mixed-signal or wireless system-on-a-chip design. The article reviews the basic performance criteria and characteristics in an easy to understand language, and describes how they affect the performance of chips.

By Adam H. Pawlikiewicz and David Hess

Over the last decade, the advances in silicon-germanium (SiGe) BiCMOS technology has been phenomenal. From its humble beginning in the late 1990s when it was looked at as nothing more than a scientific exercise at a few research labs, namely at IBM in the United States and Temic in Europe, to today where it is on the road map of every major semiconductor company. Present-day SiGe BiCMOS processes integrate high-performance heterojunction bipolar transistors (HBTs) with state-of-the-art CMOS technology. With each generation of the technology, the feature size leads to higher speeds and lower power consumption. One of the most quoted figure of merit (FoM) is the cut-off frequency - f_T , of the HBT that increased from roughly 47 GHz in the 0.5 μm generation BiCMOS process to unheard of 210 GHz in the 0.13 μm process.

Usually, the natural progression at the semiconductor companies was to develop a CMOS process first and then add more complex HBT devices that would give the needed performance for the RF applications. That combination was good when the feature sizes of 0.55 μm would give a speed of ~25 GHz on the NMOS device but around 50 GHz from the HBT device. However, with a decrease in the feature size, CMOS device speed improved enormously, as well. For instance, FoM f_T increases to more than 40 GHz at 0.18 μm feature size. With such an improvement in NMOS speeds the possibility of designing not only the logic but also the analog blocks of the RF circuits became quite obvious. The majority of today's applications could be covered with such devices. Moreover, further advances in the logic processes with the CMOS scaling pushes the mixed-signal designers toward these newer CMOS-only processes that provide the minimum speed for the application in mind.

However, the speed of the device is not the only FoM the designer has to deal with. Other specs that are as important if not more are maximum frequency of oscillation (f_{max} and $f_{\text{max,ss}}$), device transconductance (g_m), output conductance (g_o), matching, and $1/f$ noise and NF characteristics. Dynamic range is also important, along with other economic issues such as time to market, system specs and cost.

In subsequent paragraphs, we shall address these aspects from the designer's point of view. Hopefully, that discussion will help the decision makers select the optimal process for the intended application.

In the process, we shall look at the quantifiable variables such as the specs of the RF CMOS with high-quality passive devices compared to SiGe BiCMOS processes that are uniquely fit for the high-speed

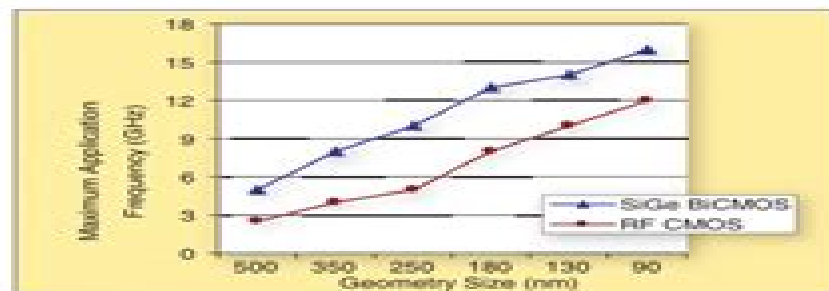


Figure 1. Maximum application frequency for CMOS and SiGe BiCMOS by transistor size (FETs).

applications. The discussion shall be centered on the high-performance SiGe BiCMOS technologies compared to the advanced CMOS technologies. It is implicitly assumed that in both cases the same number of high-quality passive elements are available. If that assumption is not met, it is not the active device performance but the quality of the passive component that might dictate the choice of the technology, since for mixed signal, or SoC designs, they are extremely important.

Technical considerations

In today's environment the choice comes down to either bipolar transistor (in BiCMOS) vs. the field effect transistor (FET) in CMOS. Moreover, since the invention of SiGe HBT, and the exponential growth in their applications, the BiCMOS process providers are almost exclusively concentrated on the SiGe BiCMOS rather than plain Si BiCMOS technologies of the past. One can start the process by comparing the electrical specs of the FET CMOS against the bipolar available in the BiCMOS process.

Historically, the shrinking of plain vanilla CMOS processes was motivated by increasing chip complexity and pricing pressures. These forces made the foundry providers shrink the device size, increase the yield and build circuits on larger wafers. With the maturity of the given logic process, and the need for even further scaling to satisfy

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