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Correct Hardware Design Methodologies: Proceedings

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Correct Hardware Design Methodologies

Lars-Henrik Eriksson, Peter A. Lindsay



Correct Hardware Design Methodologies:

Correct Hardware Design and Verification Methods George J. Milne, Laurence Pierre, 1993-05-12 These proceedings contain the papers presented at the Advanced Research Working Conference on Correct Hardware Design Methodologies held in Arles France in May 1993 and organized by the ESPRIT Working Group 6018 CHARME 2 and the Universit de Provence Marseille in cooperation with IFIP Working Group 10 2 Formal verification is emerging as a plausible alternative to exhaustive simulation for establishing correct digital hardware designs The validation of functional and timing behavior is a major bottleneck in current VLSI design systems slowing the arrival of products in the marketplace with its associated increase in cost From being a predominantly academic area of study until a few years ago formal design and verification techniques are now beginning to migrate into industrial use As we are now witnessing an increase in activity in this area in both academia and industry the aim of this working conference was to bring together researchers and users from both communities

Correct Hardware Design and Verification Methods Tiziana Margaria, Tom F. Melham, 2001-08-27 This book constitutes the refereed proceedings of the 11th IFIP WG 10 5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods CHARME 2001 held in Livingston Scotland UK in September 2001 The 28 revised full papers and eight short papers presented together with two invited papers and one special paper were carefully reviewed and selected from 56 submissions The book offers topical sections on model checking clocking issues theorem proving with higher order logics hardware compilation tools component verification case studies algorithm verification and duration calculus

Correct Hardware Design and Verification Methods Laurence Pierre, Thomas Kropf, 2003-07-31 CHARME 99 is the tenth in a series of working conferences devoted to the development and use of leading edge formal techniques and tools for the design and verification of hardware and systems Previous conferences have been held in Darmstadt 1984 Edinburgh 1985 Grenoble 1986 Glasgow 1988 Leuven 1989 Torino 1991 Arles 1993 Frankfurt 1995 and Montreal 1997 This workshop and conference series has been organized in cooperation with IFIP WG 10 5 It is now the biannual counterpart of FMCAD which takes place every even numbered year in the USA The 1999 event took place in Bad Her nalb a resort village located in the Black Forest close to the city of Karlsruhe The validation of functional and timing behavior is a major bottleneck in current VLSI design systems A predominantly academic area of study until a few years ago formal design and verification techniques are now migrating into industrial use The aim of CHARME 99 is to bring together researchers and users from academia and industry working in this active area of research Two invited talks illustrate major current trends the presentation by Gerard Berry Ecole des Mines de Paris Sophia Antipolis France is concerned with the use of synchronous languages in circuit design and the talk given by Peter Jansen BMW Munich Germany demonstrates an application of formal methods in an industrial environment The program also includes 20 regular presentations and 12 short presentations poster exhibitions that have been selected from the 48 submitted papers

Correct Hardware Design and Verification Methods

Dominique Borrione, Wolfgang Paul, 2005-10-07 This book constitutes the refereed proceedings of the 13th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods CHARME 2005 held in Saarbrücken Germany in October 2005. The 21 revised full papers and 18 short papers presented together with 2 invited talks and one tutorial were carefully reviewed and selected from 79 submissions. The papers are organized in topical sections on functional approaches to design description, game solving approaches, abstraction algorithms and techniques for speeding DD-based verification, real time and LTL model checking, evaluation of SAT based tools, model reduction and verification of memory hierarchy mechanisms. **Formal Methods in Computer-Aided Design** Mandayam Srivas, Albert

Camilleri, 1996-10-23 This book constitutes the refereed proceedings of the First International Conference on Formal Methods in Computer Aided Design FMCAD 96 held in Palo Alto California USA in November 1996. The 25 revised full papers presented were selected from a total of 65 submissions; also included are three invited survey papers and four tutorial contributions. The volume covers all relevant formal aspects of work in computer aided systems design including verification, synthesis and testing. FME 2002: Formal Methods - Getting IT Right Lars-Henrik Eriksson, Peter A. Lindsay, 2003-08-02

This volume contains the proceedings of the 2002 symposium Formal Methods in Europe FME 2002. The symposium was the 11th in a series that began with a VDM Europe symposium in 1987. The symposia are traditionally held every 18 months. In 2002 the symposium was held at the University of Copenhagen as part of the 2002 Federated Logic Conference FLoC 2002 which brought together in one event seven major conferences related to logic in computer science as well as their related workshops, tutorials and tools exhibitions. Formal Methods Europe www.fmeurope.org is an independent association which aims to stimulate the use of and research on formal methods for software development. FME symposia have been notably successful in bringing together a community of users, researchers and developers of precise mathematical methods for software development. The theme of FME 2002 was Formal Methods Getting IT Right. The double meaning was intentional. On the one hand the theme acknowledged the significant contribution formal methods can make to Information Technology by enabling computer systems to be described precisely and reasoned about with rigour. On the other hand it recognized that current formal methods are not perfect and further research and practice are required to improve their foundations, applicability and effectiveness. **Algebraic Methodology and Software Technology** Armando M. Haeberer, 2003-05-20

AMAST's goal is to advance awareness of algebraic and logical methodology as part of the fundamental basis of software technology. Ten years and seven conferences after the start of the AMAST movement I believe we are attaining this. The movement has propagated throughout the world, assembling many enthusiastic specialists who have participated not only in the conferences which are now annual but also in the innumerable other activities that AMAST promotes and supports. We are now facing the Seventh International Conference on Algebraic Methodology and Software Technology AMAST 98. The previous meetings were held in Iowa City USA 1989 and 1991 in Enschede The Netherlands 1993 in Montreal Canada 1995 in Munich Germany 1996 and in

Sydney Australia 1997 This time it is Brazil's turn in a very special part of this colorful country Amazonia Thus if we have done more it is by standing on the shoulders of giants The effort started by Teodor Rus Arthur Fleck and William A Kirk at AMAST 89 was consolidated in AMAST 91 by Teodor Rus Maurice Nivat Charles Rattray and Giuseppe Scollo Then came modular construction of the building wonderfully carried out by Giuseppe Scollo Vangalur Alagar Martin Wirsing and Michael Johnson as Program Chairs of the AMAST conferences held between 1993 and 1997 Formal Methods in Circuit Design Victoria Stavridou, 1993-07-22 Graduate level account of hardware verification and algebraic specification

Higher-Level Hardware Synthesis Richard Sharp, 2004-03-12 In the mid 1960s when a single chip contained an average of 50 transistors Gordon Moore observed that integrated circuits were doubling in complexity every year In an influential article published by Electronics Magazine in 1965 Moore predicted that this trend would continue for the next 10 years Despite being criticized for its unrealistic optimism Moore's prediction has remained valid for far longer than even he imagined today chips built using state the art techniques typically contain several million transistors The advances in fabrication technology that have supported Moore's law for four decades have fuelled the computer revolution However this exponential increase in transistor density poses new design challenges to engineers and computer scientists alike New techniques for managing complexity must be developed if circuits are to take full advantage of the vast numbers of transistors available In this monograph we investigate both i the design of high level languages for hardware description and ii techniques involved in translating these hi level languages to silicon We propose SAFL a first order functional language designed specifically for behavioral hardware description and describe the implementation of its associated silicon compiler We show that the high level properties of SAFL allow one to exploit program analyses and optimizations that are not employed in existing synthesis systems Furthermore since SAFL fully abstracts the low level details of the implementation technology we show how it can be compiled to a range of different design styles including fully synchronous design and globally asynchronous locally synchronous GALS circuits *Theorem Provers in Circuit Design* Ramayya Kumar, Thomas

Kropf, 1995-03-06 This two volume set contains papers presented at the International Conference on Computational Engineering Science ICES 95 held in Mauna Lani Hawaii from 30 July to 3 August 1995 The contributions capture the state of the science in computational modeling and simulation in a variety of engineering disciplines civil mechanical aerospace materials and electronics engineering

Architecture Design and Validation Methods Egon Börger, 2000-03-06 This state of the art survey gives a systematic presentation of recent advances in the design and validation of computer architectures The book covers a comprehensive range of architecture design and validation methods from computer aided high level design of VLSI circuits and systems to layout and testable design including the modeling and synthesis of behavior and dataflow cell based logic optimization machine assisted verification and virtual machine design **Formal Methods in**

Computer-Aided Design Ganesh Gopalakrishnan, Phillip Windley, 2003-07-31 This book constitutes the refereed

proceedings of the Second International Conference on Formal Methods in Computer Aided Design FMCAD 98 held in Palo Alto California USA in November 1998 The 27 revised full papers presented were carefully reviewed and selected from a total of 55 submissions Also included are four tools papers and four invited contributions The papers present the state of the art in formal verification methods for digital circuits and systems including processors custom VLSI circuits microcode and reactive software From the methodological point of view binary decision diagrams model checking symbolic reasoning symbolic simulation and abstraction methods are covered

Higher Order Logic Theorem Proving and Its Applications Jeffrey J. Joyce, Carl-Johan H. Seger, 1994-04-28 This volume constitutes the refereed proceedings of the 1993 Higher Order Logic Users Group Workshop held at the University of British Columbia in August 1993 The workshop was sponsored by the Centre for Integrated Computer System Research It was the sixth in the series of annual international workshops dedicated to the topic of Higher Order Logic theorem proving its usage in the HOL system and its applications The volume contains 40 papers including an invited paper by David Parnas McMaster University Canada entitled Some theorems we should prove

Perspectives of System Informatics Dines Bjørner, Manfred Broy, Igor V. Pottosin, 1996-12-04 This book constitutes the refereed post conference proceedings of the Second International Andrei Ershov Memorial Conference on System Informatics held in Akademgorodok Novosibirsk Russia in June 1996 The 27 revised full papers presented together with 9 invited contributions were thoroughly refereed for inclusion in this volume The book is divided in topical sections on programming methodology artificial intelligence natural language processing machine learning dataflow and concurrency models parallel programming supercompilation partial evaluation object oriented programming semantics and abstract interpretation programming and graphical interfaces and logic programming

Formal Methods in Computer-Aided Design Warren A. Jr. Hunt, Steven D. Johnson, 2007-11-29 The biannual Formal Methods in Computer Aided Design conference FMCAD 2000 is the third in a series of conferences under that title devoted to the use of discrete mathematical methods for the analysis of computer hardware and software The work reported in this book describes the use of modeling languages and their associated automated analysis tools to specify and verify computing systems Functional verification has become one of the principal costs in a modern computer design effort In addition verification of circuit models timing power etc requires even more effort FMCAD provides a venue for academic and industrial researchers and practitioners to share their ideas and experiences of using discrete mathematical modeling and verification It is noted with interest by the conference chairmen how this area has grown from just a few people 15 years ago to a vibrant area of research development and deployment It is clear that these methods are helping reduce the cost of designing computing systems As an example of this potential cost reduction we have invited David Russino of Advanced Micro Devices Inc to describe his verification of floating point algorithms being used in AMD microprocessors The program includes 30 regular presentations selected from 63 submitted papers

Computer Aided Verification Kim G. Larsen, 1992-04-22 This volume contains the proceedings of the

third International Workshop on Computer Aided Verification CAV 91 held in Aalborg Denmark July 1 4 1991 The objective of this series of workshops is to bring together researchers and practitioners interested in the development and use of methods tools and theories for automatic verification of finite state systems The workshop provides a unique opportunity for comparing the numerous verification methods and associated verification tools and the extent to which they may be utilized in application design The emphasis is not only on new research results but also on the application of existing results to real verification problems The papers in the volume are organized into sections on equivalence checking model checking applications tools for process algebras the state explosion problem symbolic model checking verification and transformation techniques higher order logic partial order approaches hardware verification timed specification and verification and automata

FME 2001: Formal Methods for Increasing Software Productivity Jose N. Oliveira, Pamela Zave, 2003-06-29 FME 2001 is the tenth in a series of meetings organized every eighteen months by Formal Methods Europe FME an independent association whose aim is to stimulate the use of and research on formal methods for software development It follows four VDM Europe Symposia four other Formal Methods Europe Symposia and the 1999 World Congress on Formal Methods in the Development of Computing Systems These meetings have been notably successful in bringing together a community of users researchers and developers of precise mathematical methods for software development FME 2001 took place in Berlin Germany and was organized by the Computer Science Department of the Humboldt University at Berlin The theme of the symposium was Formal Methods for Increasing Software Productivity This theme recognizes that formal methods have the potential to do more for industrial software development than enhance software quality they can also increase productivity at many different points in the software life cycle The importance of the theme is borne out by the many contributed papers showing how formal methods can make software development more efficient There is an emphasis on tools that find errors automatically or with relatively little human effort There is also an emphasis on the use of formal methods to assist with critical labor intensive tasks such as program design and test case generation

System-on-Chip Methodologies & Design Languages Peter J. Ashenden, Jean Mermet, Ralf Seepold, 2013-03-14 System on Chip Methodologies the Forum on Design Languages FDL held in Europe and the Asia Pacific Chip Design Language APChDL Conference The papers cover a range of topics including design methods specification and modeling languages tool issues formal verification simulation and synthesis The results presented in these papers will help researchers and practicing engineers keep abreast of developments in this rapidly evolving field

Formal Logical Methods for System Security and Correctness Orna Grumberg, Tobias Nipkow, Christian Pfaller, 2008 Offers information in the field of proof technology in connection with secure and correct software This title shows that methods of correct by construction program and process synthesis allow a high level programming method more amenable to security and reliability analysis and guarantees

Formal Hardware Verification Thomas Kropf, 1997-08-27 This state of the art monograph presents a coherent survey of a variety of methods and systems for

formal hardware verification It emphasizes the presentation of approaches that have matured into tools and systems usable for the actual verification of nontrivial circuits All in all the book is a representative and well structured survey on the success and future potential of formal methods in proving the correctness of circuits The various chapters describe the respective approaches supplying theoretical foundations as well as taking into account the application viewpoint By applying all methods and systems presented to the same set of IFIP WG10.5 hardware verification examples a valuable and fair analysis of the strengths and weaknesses of the various approaches is given

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