Foreword
International Conference on Multichip Modules and High Density Packaging

THIS special section of the IEEE TRANSACTIONS ON ADVANCED PACKAGING contains papers reviewed and revised from the 1998 International Conference on Multichip Modules and High Density Packaging, Denver, CO, April 15–17, 1998. These papers cover the emerging technology areas of integrated passive components, chip-scale packaging, single and multichip flip chip packages and multifunctional structures. Five additional papers addressing manufacturing related issues in electronics packaging have been selected for publication in the IEEE TRANSACTIONS ON ELECTRONICS PACKAGING MANUFACTURING.

The field of integrated passives research and development is expanding dramatically as packaging engineers realize that passive components are requiring an increasing percentage of the substrate surface area. This is particularly true of mixed signal, wireless applications. The paper by Boltan *et al.* examines high dielectric constant materials for buried capacitors in a multilayer ceramic substrate.

Chip-scale packaging (CSP) is gaining momentum as the industry pushes the boundaries in portable electronics. Itagaki *et al.* have combined ALIVH substrate technology with gold stud bump flip-chip assembly to create a new CSP. The aramid-epoxy based substrate technology uses laser-drilled holes filled with copper paste to create high-density buried vias. Stud bumping with a gold wire bonder allows use of die designed for wire bonding without additional processing. The resulting package was shown to be reliable for portable electronics application.

Jimarez *et al.* has examined the assembly and reliability of single and multichip packages. Eutectic solder flip chip and underfill was used for chip-to-package substrate assembly. Package footprints were developed to match both BGA and conventional surface mount packages such as quad flat-packs (QFP's).

In the final paper, Rawal *et al.* examine thermal management issues in multifunctional structures for spacecraft applications. Multifunctional structures integrate the electronics into the walls of the spacecraft. Thermal management is an increasingly important design issue as electronic densities continue to increase. In fact, thermal consideration may become the limiting factor in electronic density.

These papers represent approaches to addressing the challenges posed by the unrelenting demand for increasingly dense electronics. For packaging technology to keep pace with the roadmap developed by the SIA, electronics packaging research must be accelerated. Communications between researchers through conferences such as the International Conference on Multichip Modules and High Density Packaging and through the IEEE TRANSACTIONS is critical.

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R. Wayne Johnson (F'94) received the B.E. and M.Sc. degrees from Vanderbilt University, Nashville, TN, in 1979 and 1982, respectively, and the Ph.D. degree from Auburn University, Auburn, AL, in 1987, all in electrical engineering.

He has worked in the microelectronics industry for DuPont, Eaton, and Amperex. He is an Alumni Professor of electrical engineering at Auburn University and Director of the Laboratory for Electronics Assembly and Packaging (LEAP). At Auburn, he has established teaching and research laboratories for advanced packaging and electronics assembly. Research efforts are focused on materials, processing, and modeling for multichip packages and high temperature electronics. He has worked in MCM design, MCM-L, -C, and -D substrate technology as well as SMT, wire bond and flip chip assembly techniques. He has published and presented numerous papers at workshops and conferences and in technical journals. He has also co-edited one IEEE book on MCM technology and written two book chapters in the areas of silicon MCM technology and MCM assembly.

Dr. Johnson received the 1997 Auburn Alumni Engineering Council Senior Faculty Research Award for his work in electronics packaging and assembly, the 1993 John A. Wagnon, Jr. Technical Achievement Award from ISHM, and the Daniel C. Hughes Memorial Award in 1997. He is a member of SMTA and IPC, and was the 1991 President of the International Society for Hybrid Microelectronics (ISHM).

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2000 HD International Conference on High-Density Interconnect and Systems Packaging ,2000 *1998 International Conference on Multichip Modules and High Density Packaging* ,1998 Advanced Flip Chip Packaging Ho-Ming Tong,Yi-Shao Lai,C.P. Wong,2013-03-20 Advanced Flip Chip Packaging presents past present and future advances and trends in areas such as substrate technology material development and assembly processes Flip chip packaging is now in widespread use in computing communications consumer and automotive electronics and the demand for flip chip technology is continuing to grow in order to meet the need for products that offer better performance are smaller and are environmentally sustainable *Contributions from the 1998 International Conference on Multichip Modules and High Density Packaging* ,1999 **Fan-Out Wafer-Level Packaging** John H. Lau,2018-04-05 This comprehensive guide to fan out wafer level packaging FOWLP technology compares FOWLP with flip chip and fan in wafer level packaging It presents the current knowledge on these key enabling technologies for FOWLP and discusses several packaging technologies for future trends The Taiwan Semiconductor Manufacturing Company TSMC employed their InFO integrated fan out technology in A10 the application processor for Apple s iPhone in 2016 generating great excitement about FOWLP technology throughout the semiconductor packaging community For many practicing engineers and managers as well as scientists and researchers essential details of FOWLP such as the temporary bonding and de bonding of the carrier on a reconstituted wafer panel epoxy molding compound EMC dispensing compression molding Cu revealing RDL fabrication solder ball mounting etc are not well understood Intended to help readers learn the basics of problem solving methods and understand the trade offs inherent in making system level decisions quickly this book serves as a valuable reference guide for all those faced with the challenging problems created by the ever increasing interest in FOWLP helps to remove roadblocks and accelerates the design materials process and manufacturing development of key enabling technologies for FOWLP TMS 2011 140th Annual Meeting and Exhibition, Materials Fabrication, Properties, Characterization, and Modeling The Minerals, Metals & Materials Society (TMS),2011-04-12 Presents the most up to date information on the state of Materials Fabrication Properties Characterization and Modeling It s a great mix of practical applied technology and hard science which is of invaluable benefit to the global industry *Materials for Advanced Packaging* Daniel Lu,C.P. Wong,2016-11-18 Significant progress has been made in advanced packaging in recent years Several new packaging techniques have been developed and new packaging materials have been introduced This book provides a comprehensive overview of the recent developments in this industry particularly in the areas of microelectronics optoelectronics digital health and bio medical applications The book discusses established techniques as well as emerging technologies in order to provide readers with the most up to date developments in advanced packaging RF MEMS and Their Applications Vijay K. Varadan,K. J. Vinoy,K. A. Jose,2003-07-25 Microelectromechanical systems MEMS refer to a collection of micro sensors and actuators which can react to environmental change under micro circuit control The integration of MEMS into traditional Radio Frequency RF circuits has resulted in systems with superior performance levels and lower manufacturing costs The incorporation of MEMS based fabrication technologies into micro and millimeter wave systems offers viable routes to ICs with MEMS actuators antennas switches and transmission lines The resultant systems operate with an increased bandwidth and increased radiation efficiency and have considerable scope for implementation within the expanding area of wireless personal communication devices This text provides leading edge coverage of this increasingly important area and highlights the overlapping information requirements of the RF and MEMS research and development communities Provides an introduction to micromachining techniques and their use in the fabrication of micro switches capacitors and inductors Includes coverage of MEMS devices for wireless and Bluetooth enabled systems Essential reading for RF Circuit design practitioners and researchers requiring an introduction to MEMS technologies as well as practitioners and researchers in MEMS and silicon technology requiring an introduction to RF circuit design **Low Temperature Electronics and Low Temperature Cofired Ceramic Based Electronic Devices** Electrochemical Society. Meeting,2004 **Proceedings 1999 International Symposium on Microelectronics** ,1999 This text comprises the proceedings of the 1999 International Symposium on Microelectronics **Ceramic Integration and Joining Technologies** Mrityunjay Singh,Tatsuki Ohji,Rajiv Asthana,Sanjay Mathur,2011-10-11 This book joins and integrates ceramics and ceramic based materials in various sectors of technology A major imperative is to extract scientific information on joining and integration response of real as well as model material systems currently in a developmental stage This book envisions integration in its broadest sense as a fundamental enabling technology at multiple length scales that span the macro millimeter micrometer and nanometer ranges Consequently the book addresses integration issues in such diverse areas as space power and propulsion thermoelectric power generation solar energy micro electro mechanical systems MEMS solid oxide fuel cells SOFC multi chip modules prosthetic devices and implanted biosensors and stimulators The engineering challenge of designing and manufacturing complex structural functional and smart components and devices for the above applications from smaller geometrically simpler units requires innovative development of new integration technology and skillful adaptation of existing technology **Silicon Microchannel Heat Sinks** Lian Zhang,Kenneth E. Goodson,Thomas W. Kenny,2013-03-14 There is significant current interest in new technologies for IC Integrated Circuit cooling driven by the rapid increase in power densities in ICs and the trend towards high density electronic packaging for applications throughout civilian and military markets In accordance with Moore s Law the number of transistors on 6 Intel Pentium microprocessors has increased from 7 5 x10 in 1997 Pentium II to 6 55 x10 in 2002 Pentium 4 Considering the rapid increase in the integration density thermal management must be well designed to ensure proper functionality of these high speed high power chips Forced air convection has been traditionally used to remove the heat through a finned heat sink and fan module 2 Currently with 82 W power dissipation rate approximately 62 W cm heat flux from a Pentium 4 processor with 3

06 GHz core frequency the noise generated from high rotating speed fans is approaching the limit of acceptable level for humans However the power dissipation from a single cost performance chip is 2 expected to exceed 100 W cm by the year 2005 when the air cooling has to be replaced by new cooling technologies Among alternative cooling methods the two phase microchannel heat sink is one of the most promising solutions Understanding the boiling process and the two phase flow behavior in microchannels is the key to successful implementation of such a device **221** Mr. Rohit Manglik,2024-03-25 EduGorilla Publication is a trusted name in the education sector committed to empowering learners with high quality study materials and resources Specializing in competitive exams and academic support EduGorilla provides comprehensive and well structured content tailored to meet the needs of students across various streams and levels **Integrationstechnik und Aufbauarchitekturen für aktive Antennensysteme im Millimeterwellenbereich** Leif Christian Stange,2005

Advances in Embedded and Fan-Out Wafer Level Packaging Technologies Beth Keser,Steffen Kröhnert,2019-02-12 Examines the advantages of Embedded and FO WLP technologies potential application spaces package structures available in the industry process flows and material challenges Embedded and fan out wafer level packaging FO WLP technologies have been developed across the industry over the past 15 years and have been in high volume manufacturing for nearly a decade This book covers the advances that have been made in this new packaging technology and discusses the many benefits it provides to the electronic packaging industry and supply chain It provides a compact overview of the major types of technologies offered in this field on what is available how it is processed what is driving its development and the pros and cons Filled with contributions from some of the field s leading experts Advances in Embedded and Fan Out Wafer Level Packaging Technologies begins with a look at the history of the technology It then goes on to examine the biggest technology and marketing trends Other sections are dedicated to chip first FO WLP chip last FO WLP embedded die packaging materials challenges equipment challenges and resulting technology fusions Discusses specific company standards and their development results Content relates to practice as well as to contemporary and future challenges in electronics system integration and packaging Advances in Embedded and Fan Out Wafer Level Packaging Technologies will appeal to microelectronic packaging engineers managers and decision makers working in OEMs IDMs IFMs OSATs silicon foundries materials suppliers equipment suppliers and CAD tool suppliers It is also an excellent book for professors and graduate students working in microelectronic packaging research **Metal Based Thin Films for Electronics** Klaus Wetzig,Claus M. Schneider,2006-03-06 This up to date handbook covers the main topics of preparation characterization and properties of complex metal based layer systems The authors an outstanding group of researchers discuss advanced methods for structure chemical and electronic state characterization with reference to the properties of thin functional layers such as metallization and barrier layers for microelectronics magnetoresistive layers for GMR and TMR sensor and resistance layers As such the book addresses materials specialists in industry especially in microelectronics as well as scientists and can also be recommended for advanced studies in materials science analytics surface and solid state science Area Array Interconnection Handbook Karl J. Puttlitz,Paul A. Totta,2012-12-06 Microelectronic packaging has been recognized as an important enabler for the solid state revolution in electronics which we have witnessed in the last third of the twentieth century Packaging has provided the necessary external wiring and interconnection capability for transistors and integrated circuits while they have gone through their own spectacular revolution from discrete device to gigascale integration At IBM we are proud to have created the initial simple concept of flip chip with solder bump connections at a time when a better way was needed to boost the reliability and improve the manufacturability of semiconductors The basic design which was chosen for SLT Solid Logic Technology in the 1960s was easily extended to integrated circuits in the 70s and VLSI in the 80s and 90s Three I O bumps have grown to 3000 with even more anticipated for the future The package families have evolved from thick film SLT to thin film metallized ceramic to co fired multi layer ceramic A later family or ceramics with matching expansivity to sili con and copper internal wiring was developed as a predecessor of the chip interconnection revolution in copper multilevel submicron wiring Powerful server packages have been de veloped in which the combined chip and package copper wiring exceeds a kilometer All of this was achieved with the constant objective of minimizing circuit delays through short efficient interconnects **Scientific Computing in Electrical Engineering** Ursula van Rienen,Michael Günther,Dirk Hecht,2012-12-06 rd This book presents a collection of selected contributions presented at the 3 International Workshop on Scientific Computing in Electrical Engineering SCEE 2000 which took place in Warnemiinde Germany from August 20 to 23 2000 Nearly hundred scientists and engineers from thirteen countries gathered in Warnemiinde to participate in the conference Rostock Univer sity the oldest university in Northern Europe founded in 1419 hosted the conference This workshop followed two earlier workshops held 1997 at the Darmstadt University of Technology and 1998 at Weierstrass Institute for Applied Anal ysis and Stochastics in Berlin under the auspices ofthe German Mathematical Society These workshops aimed at bringing together two scientific communi ties applied mathematicians and electrical engineers who do research in the field of scientific computing in electrical engineering This of course is a wide field which is why it was decided to concentrate on selected major topics The workshop in Darmstadt which was organized by Michael Giinther from the Mathematics Department and Ursula van Rienen from the Department of Electrical Engineering and Information Technology brought together more than hundred scientists interested in numerical methods for the simulation of circuits and electromagnetic fields This was a great success Voices coming from the participants suggested that it was time to bring these communities together in order to get to know each other to discuss mutual interests and to start cooperative work A collection of selected contributions appeared in Surveys on Mathematics for Industry Vol 8 No 3 4 and Vol 9 No 2 1999

System-in-Package Lei He,Shauki Elassaad,Yiyu Shi,Yu Hu,Wei Yao,2011-06-20 Surveys the electrical and layout perspectives of System in Package the system integration technology that has emerged as a required technology to reduce the system board space and height in addition to the overall time to market and design cost of consumer electronics products such as those of cell phones audio video players and digital cameras **Encyclopedia Of Packaging Materials, Processes, And Mechanics - Set 1: Die-attach And Wafer Bonding Technology (A 4-volume Set)** ,2019-08-27 Packaging materials assembly processes and the detailed understanding of multilayer mechanics have enabled much of the progress in miniaturization reliability and functional density achieved by modern electronic microelectronic and nanoelectronic products The design and manufacture of miniaturized packages providing low loss electrical and or optical communication while protecting the semiconductor chips from environmental stresses and internal power cycling require a carefully balanced selection of packaging materials and processes Due to the relative fragility of these semiconductor chips as well as the underlying laminated substrates and the bridging interconnect selection of the packaging materials and processes is inextricably bound with the mechanical behavior of the intimately packaged multilayer structures in all phases of development for traditional as well as emerging electronic product categories The Encyclopedia of Packaging Materials Processes and Mechanics compiled in 8 multi volume sets provides comprehensive coverage of the configurations and techniques assembly materials and processes modeling and simulation tools and experimental characterization and validation techniques for electronic packaging Each of the volumes presents the accumulated wisdom and shared perspectives of leading researchers and practitioners in the packaging of electronic components The Encyclopedia of Packaging Materials Processes and Mechanics will provide the novice and student with a complete reference for a quick ascent on the packaging learning curve the practitioner with a validated set of techniques and tools to face every challenge in packaging design and development and researchers with a clear definition of the state of the art and emerging needs to guide their future efforts This encyclopedia will thus be of great interest to packaging engineers electronic product development engineers and product managers as well as to researchers in the assembly and mechanical behavior of electronic and photonic components and systems It will be most beneficial to undergraduate and graduate students studying materials mechanical electrical and electronic engineering with a strong interest in electronic packaging applications

The Enigmatic Realm of **1998 International Conference On Multichip Modules And High Density Packaging**: Unleashing the Language is Inner Magic

In a fast-paced digital era where connections and knowledge intertwine, the enigmatic realm of language reveals its inherent magic. Its capacity to stir emotions, ignite contemplation, and catalyze profound transformations is nothing in short supply of extraordinary. Within the captivating pages of **1998 International Conference On Multichip Modules And High Density Packaging** a literary masterpiece penned by a renowned author, readers embark on a transformative journey, unlocking the secrets and untapped potential embedded within each word. In this evaluation, we shall explore the book is core themes, assess its distinct writing style, and delve into its lasting impact on the hearts and minds of those that partake in its reading experience.

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