

Defect and Fault Tolerance in VLSI Systems

Edited by
Israel Koren

Defect And Fault Tolerance In Vlsi Systems Proceedings

Israel Koren



Defect And Fault Tolerance In Vlsi Systems Proceedings:

Defect and Fault Tolerance in VLSI Systems IEEE Computer Society, 1993 *Proceedings ... IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, 1996 *Defect and Fault-Tolerance in VLSI Systems* IEEE Computer Society, 1999-11-01 *Defect and Fault Tolerance in VLSI Systems: Proceedings of the International Symposium, Albuquerque, New Mexico, 1999* IEEE Staff, 1999 **Fault Tolerant Computer Architecture** Daniel Sorin, 2022-05-31 For many years most computer architects have pursued one primary goal performance Architects have translated the ever increasing abundance of ever faster transistors provided by Moore s law into remarkable increases in performance Recently however the bounty provided by Moore s law has been accompanied by several challenges that have arisen as devices have become smaller including a decrease in dependability due to physical faults In this book we focus on the dependability challenge and the fault tolerance solutions that architects are developing to overcome it The two main purposes of this book are to explore the key ideas in fault tolerant computer architecture and to present the current state of the art over approximately the past 10 years in academia and industry Table of Contents Introduction Error Detection Error Recovery Diagnosis Self Repair The Future **Defect and Fault Tolerance in VLSI Systems**, 1998 *Proceedings, 1992 IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems* Duncan Moore Henry Walker, Fabrizio Lombardi, 1992 *Defect and Fault Tolerance in VLSI Systems: Proceedings* Dimitris Gizopoulos, et al, 2009

Proceedings, 1997 *Software-Implemented Hardware Fault Tolerance* Olga Goloubeva, Maurizio Rebaudengo, Matteo Sonza Reorda, Massimo Violante, 2006-09-19 Software Implemented Hardware Fault Tolerance addresses the innovative topic of software implemented hardware fault tolerance SIHFT i e how to deal with faults affecting the hardware by only or mainly acting on the software The first SIHFT techniques were proposed and adopted several decades ago but they have been the object of new interest in the past few years mainly due to the need for developing low cost safety critical computer based applications in fields such as automotive biomedics and telecommunications Therefore several new approaches to detect and when possible correct transient and permanent faults in the hardware have been recently proposed These approaches are innovative with respect to those proposed in the past since they are of higher applicability often starting from the source level code of an application and generality being capable of coping with many different fault types The book presents the theory behind software implemented hardware fault tolerance as well as the practical aspects related to put it at work on real examples By evaluating accurately the advantages and disadvantages of the already available approaches the book provides a guide to developers willing to adopt software implemented hardware fault tolerance in their applications Moreover the book identifies open issues for researchers willing to improve the already available techniques **Defect and Fault Tolerance in VLSI Systems** Israel Koren, Charles H. Stapper, International Workshop on Defect and Fault Tolerance in VLSI Systems (1988, Springfield, Mass.), 1990 **Reliability of Nanoscale Circuits and Systems** Miloš

Stanisavljević, Alexandre Schmid, Yusuf Leblebici, 2010-10-20 This book is intended to give a general overview of reliability faults fault models nanotechnology nanodevices fault tolerant architectures and reliability evaluation techniques Additionally the book provides an in depth state of the art research results and methods for fault tolerance as well as the methodology for designing fault tolerant systems out of highly unreliable components **Energy-Efficient Fault-Tolerant Systems** Jimson Mathew, Rishad A. Shafik, Dhiraj K. Pradhan, 2013-09-07 This book describes the state of the art in energy efficient fault tolerant embedded systems It covers the entire product lifecycle of electronic systems design analysis and testing and includes discussion of both circuit and system level approaches Readers will be enabled to meet the conflicting design objectives of energy efficiency and fault tolerance for reliability given the up to date techniques presented Defect and Fault Tolerance in VLSI Systems Israel Koren, 1989 Defect and Fault Tolerance in VLSI Systems Israel Koren, 1989-08-01 This book contains an edited selection of papers presented at the International Workshop on Defect and Fault Tolerance in VLSI Systems held October 6 7 1988 in Springfield Massachusetts Our thanks go to all the contributors and especially the members of the program committee for the difficult and time consuming work involved in selecting the papers that were presented in the workshop and reviewing the papers included in this book Thanks are also due to the IEEE Computer Society in particular the Technical Committee on Fault Tolerant Computing and the Technical Committee on VLSI and the University of Massachusetts at Amherst for sponsoring the workshop and to the National Science Foundation for supporting under grant number MIP 8803418 the keynote address and the distribution of this book to all workshop attendees The objective of the workshop was to bring together researchers and practitioners from both industry and academia in the field of defect tolerance and yield enhancement in VLSI to discuss their mutual interests in defect tolerant architectures and models for integrated circuit defects faults and yield Progress in this area was slowed down by the proprietary nature of yield related data and by the lack of appropriate forums for disseminating such information The goal of this workshop was therefore to provide a forum for a dialogue and exchange of views A follow up workshop in October 1989 with C H Stapper from IBM and V K Jain from the University of South Florida as general co chairmen is being organized **Design of Semiconductor QCA Systems** Weiqiang Liu, Earl E. Swartzlander Jr., Máire O'Neill, 2013-10-01 Integrated circuits have become smaller cheaper and more reliable and certainly have revolutionized the world of electronics Integrated circuits are used in almost all electronic devices and systems many of which such as the Internet computers and mobile phones have become essential parts of modern life and have changed the way we live Quantum dot cellular automata QCA provides a revolutionary approach to computing with device to device interactions The design of a QCA circuit is radically different from a conventional digital design due to its unique characteristics at both the physical level and logic level Research on both circuit architecture and device design is required for a profound understanding of QCA nanotechnologies This detailed reference presents practical design aspects of QCA with an emphasis on developing real world implementations *Proceedings, the*

IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems, November 13-15, 1995, Lafayette, Louisiana
IEEE Computer Society, 1995 An invited talk recounts Intel's experience with increasing die yield through CAD algorithms and a panel discussion examines tools for the extracting of critical areas for a yield analysis of VLSI design Others of the 34 papers cover critical area analysis defect sensitivity and reliability fault tolerant architectures and arrays yield projection and enhancement fault tolerant and testing techniques and self checking and coding techniques No subject index Annotation copyright by Book News Inc Portland OR

Hybrid Fault Tolerance Techniques to Detect Transient Faults in Embedded Processors José Rodrigo Azambuja, Fernanda Kastensmidt, Jürgen Becker, 2014-07-07 This book describes fault tolerance techniques based on software and hardware to create hybrid techniques They are able to reduce overall performance degradation and increase error detection when associated with applications implemented in embedded processors Coverage begins with an extensive discussion of the current state of the art in fault tolerance techniques The authors then discuss the best trade off between software based and hardware based techniques and introduce novel hybrid techniques Proposed techniques increase existing fault detection rates up to 100% while maintaining low performance overheads in area and application execution time

Soft Errors in Modern Electronic Systems Michael Nicolaidis, 2010-09-24 This book provides a comprehensive presentation of the most advanced research results and technological developments enabling understanding qualifying and mitigating the soft errors effect in advanced electronics including the fundamental physical mechanisms of radiation induced soft errors the various steps that lead to a system failure the modelling and simulation of soft error at various levels including physical electrical netlist event driven RTL and system level modelling and simulation hardware fault injection accelerated radiation testing and natural environment testing soft error oriented test structures process level device level cell level circuit level architectural level software level and system level soft error mitigation techniques The book contains a comprehensive presentation of most recent advances on understanding qualifying and mitigating the soft error effect in advanced electronic systems presented by academia and industry experts in reliability fault tolerance EDA processor SoC and system design and in particular experts from industries that have faced the soft error impact in terms of product reliability and related business issues and were in the forefront of the countermeasures taken by these companies at multiple levels in order to mitigate the soft error effects at a cost acceptable for commercial products In a fast moving field where the impact on ground level electronics is very recent and its severity is steadily increasing at each new process node impacting one after another various industry sectors as an example the Automotive Electronics Council comes to publish qualification requirements on soft errors research and technology developments and industrial practices have evolve very fast outdating the most recent books edited at 2004

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Whispering the Strategies of Language: An Mental Journey through **Defect And Fault Tolerance In Vlsi Systems Proceedings**

In a digitally-driven earth wherever displays reign great and quick conversation drowns out the subtleties of language, the profound secrets and emotional nuances concealed within phrases usually go unheard. However, set within the pages of **Defect And Fault Tolerance In Vlsi Systems Proceedings** a fascinating fictional value blinking with organic emotions, lies an extraordinary journey waiting to be undertaken. Published by a talented wordsmith, this charming opus encourages viewers on an introspective trip, gently unraveling the veiled truths and profound impact resonating within the fabric of each word. Within the emotional depths with this moving review, we will embark upon a honest exploration of the book is primary themes, dissect its fascinating publishing model, and yield to the powerful resonance it evokes heavy within the recesses of readers hearts.

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