
Verification (digital): ASICs and FPGAs

Getting ASIC right first time.

Get large complex FPGA based systems working

Asic And Fpga Verification

Xiaohua Tian, Thinh M. Le, Yong Lian

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ASIC and FPGA Verification Richard Munden, 2004-10-23 Richard Munden demonstrates how to create and use simulation models for verifying ASIC and FPGA designs and board level designs that use off the shelf digital components Based on the VHDL VITAL standard these models include timing constraints and propagation delays that are required for accurate verification of today s digital designs ASIC and FPGA Verification A Guide to Component Modeling expertly illustrates how ASICs and FPGAs can be verified in the larger context of a board or a system It is a valuable resource for any designer who simulates multi chip digital designs Provides numerous models and a clearly defined methodology for performing board level simulation Covers the details of modeling for verification of both logic and timing First book to collect and teach techniques for using VHDL to model off the shelf or IP digital components for use in FPGA and board level design verification

Writing Testbenches using SystemVerilog Janick Bergeron, 2007-02-02 Verification is too often approached in an ad hoc fashion Visually inspecting simulation results is no longer feasible and the directed test case methodology is reaching its limit Moore s Law demands a productivity revolution in functional verification methodology Writing Testbenches Using SystemVerilog offers a clear blueprint of a verification process that aims for first time success using the SystemVerilog language From simulators to source management tools from specification to functional coverage from I s and O s to high level abstractions from interfaces to bus functional models from transactions to self checking testbenches from directed testcases to constrained random generators from behavioral models to regression suites this book covers it all Writing Testbenches Using SystemVerilog presents many of the functional verification features that were added to the Verilog language as part of SystemVerilog Interfaces virtual modports classes program blocks clocking blocks and others SystemVerilog features are introduced within a coherent verification methodology and usage model Writing Testbenches Using SystemVerilog introduces the reader to all elements of a modern scalable verification methodology It is an introduction and prelude to the verification methodology detailed in the Verification Methodology Manual for SystemVerilog It is a SystemVerilog version of the author s bestselling book Writing Testbenches Functional Verification of HDL Models

Getting Started with FPGAs Russell Merrick, 2023-11-21 Skip the complexity and learn to program FPGAs the easy way through this hands on beginner friendly introduction to digital circuit design with Verilog and VHDL Whether you have been toying with field programmable gate arrays FPGAs for years or are completely new to these reprogrammable devices this book will teach you to think like an FPGA engineer and develop reliable designs with confidence Through detailed code examples patient explanations and hands on projects Getting Started with FPGAs will actually get you started Russell Merrick creator of the popular blog Nandland com will guide you through the basics of digital logic look up tables and flip flops as well as high level concepts like state machines You ll explore the fundamentals of the FPGA build process including simulation synthesis and place and route You ll learn about key FPGA primitives such as DSP blocks and PLLs and examine

how FPGAs handle math operations and I O Code examples are provided in both Verilog and VHDL making the book a valuable resource no matter your language of choice You ll discover how to Implement common design building blocks like multiplexers LFSRs and FIFOs Cross between clock domains without triggering metastable conditions or timing errors Avoid common pitfalls when performing math Transmit and receive data at lightning speeds using SerDes Write testbench code to verify your designs are working With this accessible hands on guide you ll be creating your own functional FPGA projects in no time Getting started with FPGAs has never been easier *Writing Testbenches: Functional Verification of HDL Models* Janick Bergeron, 2012-12-06 mental improvements during the same period What is clearly needed in verification techniques and technology is the equivalent of a synthesis productivity breakthrough In the second edition of *Writing Testbenches* Bergeron raises the verification level of abstraction by introducing coverage driven constrained random transaction level self checking testbenches all made possible through the introduction of hardware verification languages HVLs such as e from Verisity and OpenVera from Synopsys The state of art methodologies described in *Writing Test benches* will contribute greatly to the much needed equivalent of a synthesis breakthrough in verification productivity I not only highly recommend this book but also I think it should be required reading by anyone involved in design and verification of today s ASIC SoCs and systems Harry Foster Chief Architect Verplex Systems Inc xviii *Writing Testbenches Functional Verification of HDL Models* PREFACE If you survey hardware design groups you will learn that between 60% and 80% of their effort is now dedicated to verification **Timing Verification of Application-specific Integrated Circuits (ASICs)** Farzad Nekoogar, 1999 PLEASE PROVIDE COURSE INFORMATION PLEASE PROVIDE *Embedded Systems and Software Validation* Abhik Roychoudhury, 2009-04-29 Modern embedded systems require high performance low cost and low power consumption Such systems typically consist of a heterogeneous collection of processors specialized memory subsystems and partially programmable or fixed function components This heterogeneity coupled with issues such as hardware software partitioning mapping scheduling etc leads to a large number of design possibilities making performance debugging and validation of such systems a difficult problem Embedded systems are used to control safety critical applications such as flight control automotive electronics and healthcare monitoring Clearly developing reliable software systems for such applications is of utmost importance This book describes a host of debugging and verification methods which can help to achieve this goal Covers the major abstraction levels of embedded systems design starting from software analysis and micro architectural modeling to modeling of resource sharing and communication at the system level Integrates formal techniques of validation for hardware software with debugging and validation of embedded system design flows Includes practical case studies to answer the questions does a design meet its requirements if not then which parts of the system are responsible for the violation and once they are identified then how should the design be suitably modified **Integrated Circuit Design** Xiaokun Yang, 2024-11-20 This textbook seeks to foster a deep understanding of the field by introducing the industry

integrated circuit IC design flow and offering tape out or pseudo tape out projects for hands on practice facilitating project based learning PBL experiences Integrated Circuit Design IC Design Flow and Project Based Learning aims to equip readers for entry level roles as IC designers in the industry and as hardware design researchers in academia The book commences with an overview of the industry IC design flow with a primary focus on register transfer level RTL design the automation of simulation and verification and system on chip SoC integration To build connections between RTL design and physical hardware FPGA field programmable gate array synthesis and implementation is utilized to illustrate the hardware description and performance evaluation The second objective of this book is to provide readers with practical hands on experience through tape out or pseudo tape out experiments labs and projects These activities are centered on coding format industry design rules synthesizable Verilog designs clock domain crossing etc and commonly used bus protocols arbitration handshaking etc as well as established design methodologies for widely adopted hardware components including counters timers finite state machines FSMs I2C single dual port and ping pong buffers register files FIFOs floating point units FPU's numerical hardware Fourier transform matrix matrix multiplication etc direct memory access DMA image processing designs neural networks and more The textbook caters to a diverse readership including junior and senior undergraduate students as well as graduate students pursuing degrees in electrical engineering computer engineering computer science and related fields The target audience is expected to have a basic understanding of Boolean Algebra and Karnaugh Maps as well as prior familiarity with digital logic components such as AND OR gates latches and flip flops The book will also be useful for entry level RTL designers and verification engineers who are embarking on their journey in application specific IC ASIC and FPGA design industry

Writing Testbenches Janick Bergeron, 2007-05-08 CHAPTER 6 Architecting Testbenches 221 Reusable Verification Components 221 Procedural Interface 225 Development Process 226 Verilog Implementation 227 Packaging Bus Functional Models 228 Utility Packages 231 VHDL Implementation 237 Packaging Bus Functional Procedures 238 240 Creating a Test Harness 243 Abstracting the Client Server Protocol Managing Control Signals 246 Multiple Server Instances 247 Utility Packages 249 Autonomous Generation and Monitoring 250 Autonomous Stimulus 250 Random Stimulus 253 Injecting Errors 255 Autonomous Monitoring 255 258 Autonomous Error Detection Input and Output Paths 258 Programmable Testbenches 259 Configuration Files 260 Concurrent Simulations 261 Compile Time Configuration 262 Verifying Configurable Designs 263 Configurable Testbenches 265 Top Level Generics and Parameters 266 Summary 268 CHAPTER 7 Simulation Management 269 Behavioral Models 269 Behavioral versus Synthesizable Models 270 Example of Behavioral Modeling 271 Characteristics of a Behavioral Model 273 x Writing Testbenches Functional Verification of HDL Models Modeling Reset 276 Writing Good Behavioral Models 281 Behavioral Models Are Faster 285 The Cost of Behavioral Models 286 The Benefits of Behavioral Models 286 Demonstrating Equivalence 289 Pass or Fail 289 Managing Simulations 292 294 Configuration Management Verilog Configuration Management 295 VHDL Configuration Management 301 SDF

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Low-Power Design of Nanometer FPGAs Hassan Hassan, Mohab Anis, 2009-09-14 Low Power Design of Nanometer FPGAs Architecture and EDA is an invaluable reference for researchers and practicing engineers concerned with power efficient FPGA design State of the art power reduction techniques for FPGAs will be described and compared These techniques can be applied at the circuit architecture and electronic design automation levels to describe both the dynamic and leakage power sources and enable strategies for codesign Low power techniques presented at key FPGA design levels for circuits architectures and electronic design automation form critical bridge guidelines for codesign Comprehensive review of leakage tolerant techniques empowers designers to minimize power dissipation Provides valuable tools for estimating power efficiency savings of current low power FPGA design techniques **Heterogeneous SoC Design and Verification** Khaled Salah Mohamed, 2024-03-22 This book covers the foundations of hardware software codesign on chip communication debugging and verification for heterogeneous SoCs Its primary objective is to empower designers in making informed decisions guiding them to strike the perfect balance between flexibility and performance for their SoC designs Readers will benefit from a detailed exploration of the essential elements of the hardware and software codesign framework accompanied by a discussion of the driving motivations behind this approach The author also provides an in depth review of various hardware design architectures shedding light on different design possibilities Furthermore the book presents key concepts concerning hardware and software communication unraveling the intricate interactions within an SoC This book provides a holistic introduction to the methodologies underpinning SoC design and verification making it an indispensable companion for both novice and experienced designers navigating the ever evolving landscape of hardware software codesign

FPGAs: World Class Designs Clive Maxfield, 2009-02-24 All the design and development inspiration and direction a hardware engineer needs in one blockbuster book Clive Maxfield renowned author columnist and editor of PL DesignLine has selected the very best FPGA design material from the Newnes portfolio and has compiled it into this volume The result is a book covering the gamut of FPGA design from design fundamentals to optimized layout techniques with a strong pragmatic emphasis In addition to specific design techniques and practices this book also discusses various approaches to solving FPGA design problems and how to successfully apply theory to actual design tasks The material has been selected for its timelessness as well as for its relevance to contemporary FPGA design issues Contents Chapter 1 Alternative FPGA Architectures Chapter 2 Design Techniques Rules and Guidelines Chapter 3 A VHDL Primer The Essentials Chapter 4 Modeling Memories Chapter 5 Introduction to Synchronous State Machine Design and Analysis Chapter 6 Embedded Processors Chapter

7 Digital Signal ProcessingChapter 8 Basics of Embedded Audio ProcessingChapter 9 Basics of Embedded Video and Image ProcessingChapter 10 Programming Streaming FPGA Applications Using Block Diagrams In SimulinkChapter 11 Ladder and functional block programmingChapter 12 Timers Hand picked content selected by Clive Max Maxfield character luminary columnist and author Proven best design practices for FPGA development verification and low power Case histories and design examples get you off and running on your current project

DCIS2002 Salvador Bracho del Pino,Mar Martínez,Teresa Riesgo,Miguel Ángel Allende Recio,2002 Este libro contiene las presentaciones de la XVII Conferencia de Dise ñ o de Circuitos y Sistemas Integrados celebrado en el Palacio de la Magdalena Santander en noviembre de 2002 Esta Conferencia ha alcanzado un alto nivel de calidad como consecuencia de su tradici ñ y madurez que lo convierte en uno de los acontecimientos m s importantes para los circuitos de microelectr ñ ica y la comunidad de dise ñ o de sistemas en el sur de Europa Desde su origen tiene una gran contribuci ñ de Universidades espa ñ olas aunque hoy los autores participan desde catorce pa ses

Logic Synthesis and SOC Prototyping Vaibbhav Taraate,2020-01-03 This book describes RTL design synthesis and timing closure strategies for SOC blocks It covers high level RTL design scenarios and challenges for SOC design The book gives practical information on the issues in SOC and ASIC prototyping using modern high density FPGAs The book covers SOC performance improvement techniques testing and system level verification The book also describes the modern Xilinx FPGA architecture and their use in SOC prototyping The book covers the Synopsys DC PT commands and use of them to constraint and to optimize SOC design The contents of this book will be of use to students professionals and hobbyists alike

Quantifying and Exploring the Gap Between FPGAs and ASICs Ian Kuon,Jonathan Rose,2010-07-03 Field programmable gate arrays FPGAs which are pre fabricated programmable digital integrated circuits ICs provide easy access to state of the art integrated circuit process technology and in doing so democratize this technology of our time This book is about comparing the qualities of FPGA their speed performance area and power consumption against custom fabricated ICs and exploring ways of mitigating their de ciencias This work began as a question that many have asked and few had the resources to answer how much worse is an FPGA compared to a custom designed chip As we dealt with that question we found that it was far more dif cult to answer than we anticipated but that the results were rich basic insights on fundamental understandings of FPGA architecture It also encouraged us to nd ways to leverage those insights to seek ways to make FPGA technology better which is what the second half of the book is about While the question How much worse is an FPGA than an ASIC has been a constant sub theme of all research on FPGAs it was posed most directly some time around May 2004 by Professor Abbas El Gamal from Stanford University to us he was working on a 3D FPGA and was wondering if any real measurements had been made in this kind of comparison Shortly thereafter we took it up and tried to answer in a serious way

Embedded Software: Know It All Jean J. Labrosse,2007-09-14 Embedded software is present everywhere from a garage door opener to implanted medical devices to multicore computer systems This book covers the development and

testing of embedded software from many different angles and using different programming languages *Entropy Coders of the H.264/AVC Standard* Xiaohua Tian, Thinh M. Le, Yong Lian, 2010-10-17 This book presents a collection of algorithms and VLSI architectures of entropy or statistical codecs of recent video compression standards with focus on the H 264 AVC standard For any visual data compression scheme there exists a combination of two or all of the following three stages spatial temporal and statistical compression General readers are first introduced with the various algorithms of the statistical coders The VLSI implementations are also reviewed and discussed Readers with limited hardware design background are also introduced with a design methodology starting from performance complexity analyses to software hardware co simulation A typical design of the Contextbased Adaptive Binary Arithmetic Coding CABAC encoder is also presented in details To support System on Chip design environment the CABAC design is wrapped with a SoC based Wishbone system bus interface

Designing with FPGAs and CPLDs Bob Zeidman, 2002-01-09 Choose the right programmable logic devices and development tools Understand the design verification and testing issues Plan schedules and allocate resources efficiently Choose the right programmable logic devices with this guide to the technology *100 Power Tips for FPGA Designers* ,

Principles of Verilog Digital Design Wen-Long Chin, 2022-02-27 Covering both the fundamentals and the in depth topics related to Verilog digital design both students and experts can benefit from reading this book by gaining a comprehensive understanding of how modern electronic products are designed and implemented Principles of Verilog Digital Design contains many hands on examples accompanied by RTL codes that together can bring a beginner into the digital design realm without needing too much background in the subject area This book has a particular focus on how to transform design concepts into physical implementations using architecture and timing diagrams Common mistakes a beginner or even an experienced engineer can make are summarized and addressed as well Beyond the legal details of Verilog codes the book additionally presents what uses Verilog codes have through some pertinent design principles Moreover students reading this book will gain knowledge about system level design concepts Several ASIC designs are illustrated in detail as well In addition to design principles and skills modern design methodology and how it is carried out in practice today are explored in depth as well

FPGA Design Philip Simpson, 2010-07-23 In August of 2006 an engineering VP from one of Altera s customers approached Misha Burich VP of Engineering at Altera asking for help in reliably being able to predict the cost schedule and quality of system designs reliant on FPGA designs At this time I was responsible for defining the design flow requirements for the Altera design software and was tasked with investigating this further As I worked with the customer to understand what worked and what did not work reliably in their FPGA design process I noted that this problem was not unique to this one customer The characteristics of the problem are shared by many Corporations that implement designs in FPGAs The Corporation has many design teams at different locations and the success of the FPGA projects vary between the teams There is a wide range of design experience across the teams There is no working process for sharing design blocks between

engineering teams As I analyzed the data that I had received from hundreds of customer visits in the past I noticed that design reuse among engineering teams was a challenge I also noticed that many of the design teams at the same Companies and even within the same design team used different design methodologies Altera had recently solved this problem as part of its own FPGA design software and IP development process

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