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Heterogeneous Memory Organizations in Embedded Systems Miguel Peón Quirós,Francky Catthoor,José Manuel Mendías Cuadros,2020-01-30 This book defines and explores the problem of placing the instances of dynamic data types on the components of the heterogeneous memory organization of an embedded system with the final goal of reducing energy consumption and improving performance It is one of the first to cover the problem of placement for dynamic data objects on embedded systems with heterogeneous memory architectures presenting a complete methodology that can be easily adapted to real cases and work flows The authors discuss how to improve system performance and energy consumption simultaneously Discusses the problem of placement for dynamic data objects on embedded systems with heterogeneous memory architectures Presents a complete methodology that can be adapted easily to real cases and work flows Offers hints on how to improve system performance and energy consumption simultaneously   VLSI Design and Test for Systems Dependability Shojiro Asai,2018-07-20 This book discusses the new roles that the VLSI very large scale integration of semiconductor circuits is taking for the safe secure and dependable design and operation of electronic systems The book consists of three parts Part I as a general introduction to this vital topic describes how electronic systems are designed and tested with particular emphasis on dependability engineering where the simultaneous assessment of the detrimental outcome of failures and cost of their containment is made This section also describes the related research project Dependable VLSI Systems in which the editor and authors of the book were involved for 8 years Part II addresses various threats to the dependability of VLSIs as key systems components including time dependent degradations variations in device characteristics ionizing radiation electromagnetic interference design errors and tampering with discussion of technologies to counter those threats Part III elaborates on the design and test technologies for dependability in such applications as control of robots and vehicles data processing and storage in a cloud environment and heterogeneous wireless telecommunications This book is intended to be used as a reference for engineers who work on the design and testing of VLSI systems with particular attention to dependability It can be used as a textbook in graduate courses as well Readers interested in dependable systems from social and industrial economic perspectives will also benefit from the discussions in this book   *Applied Formal Methods - FM-Trends 98* Dieter Hutter,Werner Stephan,Paolo Traverso,Markus Ullmann,2007-07-21 This volume contains the contributions presented at the International Workshop on Current Trends in Applied Formal Methods organized October 7 9 1998 in Boppard Germany The main objective of the workshop was to draw a map of the key issues facing the practical application of formal methods in industry This appears to be particularly timely with safety and security issues becoming a real obstacle to industrial software and hardware development As a consequence almost all major companies have now set up departments or groups to work with formal methods and many European countries face a severe labour shortage in this new field Tony Hoare s prediction of the art of software and hardware

development becoming a proper engineering science with its own body of tools and techniques is now becoming a reality So the focus of this application oriented workshop was not so much on spe cial academic topics but rather on the many practical aspects of this emerging new technology verification and validation and tool support and integration into the software life cycle By evaluating the state of the art with respect to industrial applications a discussion emerged among scientists practising engi neers and members of regulatory and funding agencies about future needs and developments This discussion lead to roadmaps with respect to the future of this field to tool support and potential application areas and promising market segments The contributions of the participants from industry as well as from the respective national security bureaus were particularly valuable and highly appreciated **Low-Power High-Level Synthesis for Nanoscale CMOS Circuits** Saraju P. Mohanty,Nagarajan Ranganathan,Elias Kougianos,Priyardarsan Patra,2008-05-31 Low Power High Level Synthesis for Nanoscale CMOS Circuits addresses the need for analysis characterization estimation and optimization of the various forms of power dissipation in the presence of process variations of nano CMOS technologies The authors show very large scale integration VLSI researchers and engineers how to minimize the different types of power consumption of digital circuits The material deals primarily with high level architectural or behavioral energy dissipation because the behavioral level is not as highly abstracted as the system level nor is it as complex as the gate transistor level At the behavioral level there is a balanced degree of freedom to explore power reduction mechanisms the power reduction opportunities are greater and it can cost effectively help in investigating lower power design alternatives prior to actual circuit layout or silicon implementation The book is a self contained low power high level synthesis text for Nanoscale VLSI design engineers and researchers Each chapter has simple relevant examples for a better grasp of the principles presented Several algorithms are given to provide a better understanding of the underlying concepts The initial chapters deal with the basics of high level synthesis power dissipation mechanisms and power estimation In subsequent parts of the text a detailed discussion of methodologies for the reduction of different types of power is presented including Power Reduction Fundamentals Energy or Average Power Reduction Peak Power Reduction Transient Power Reduction Leakage Power Reduction Low Power High Level Synthesis for Nanoscale CMOS Circuits provides a valuable resource for the design of low power CMOS circuits

Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication Shen, Jih-Sheng,Hsiung, Pao-Ann,2010-06-30 Reconfigurable computing brings immense flexibility to on chip processing while network on chip has improved flexibility in on chip communication Integrating these two areas of research reaps the benefits of both and represents the promising future of multiprocessor systems on chip This book is the one of the first compilations written to demonstrate this future for network on chip design Through dynamic and creative research into questions ranging from integrating reconfigurable computing techniques to task assigning scheduling and arrival to designing an operating system to take advantage of the computing and communication flexibilities brought about by run time reconfiguration and

network on chip it represents a complete source of the techniques and applications for reconfigurable network on chip necessary for understanding of future of this field *Secure System Design and Trustable Computing* Chip-Hong Chang,Miodrag Potkonjak,2015-09-17 This book provides the foundations for understanding hardware security and trust which have become major concerns for national security over the past decade Coverage includes issues related to security and trust in a variety of electronic devices and systems related to the security of hardware firmware and software spanning system applications online transactions and networking services This serves as an invaluable reference to the state of the art research that is of critical significance to the security of and trust in modern society s microelectronic supported infrastructures On-Chip Communication Architectures Sudeep Pasricha,Nikil Dutt,2010-07-28 Over the past decade system on chip SoC designs have evolved to address the ever increasing complexity of applications fueled by the era of digital convergence Improvements in process technology have effectively shrunk board level components so they can be integrated on a single chip New on chip communication architectures have been designed to support all inter component communication in a SoC design These communication architecture fabrics have a critical impact on the power consumption performance cost and design cycle time of modern SoC designs As application complexity strains the communication backbone of SoC designs academic and industrial R D efforts and dollars are increasingly focused on communication architecture design On Chip Communication Architecures is a comprehensive reference on concepts research and trends in on chip communication architecture design It will provide readers with a comprehensive survey not available elsewhere of all current standards for on chip communication architectures A definitive guide to on chip communication architectures explaining key concepts surveying research efforts and predicting future trends Detailed analysis of all popular standards for on chip communication architectures Comprehensive survey of all research on communication architectures covering a wide range of topics relevant to this area spanning the past several years and up to date with the most current research efforts Future trends that with have a significant impact on research and design of communication architectures over the next several years **Adaptable Embedded Systems** Antonio Carlos Schneider Beck,Carlos Arthur Lang Lisbôa,Luigi Carro,2012-11-27 As embedded systems become more complex designers face a number of challenges at different levels they need to boost performance while keeping energy consumption as low as possible they need to reuse existent software code and at the same time they need to take advantage of the extra logic available in the chip represented by multiple processors working together This book describes several strategies to achieve such different and interrelated goals by the use of adaptability Coverage includes reconfigurable systems dynamic optimization techniques such as binary translation and trace reuse new memory architectures including homogeneous and heterogeneous multiprocessor systems communication issues and NOCs fault tolerance against fabrication defects and soft errors and finally how one can combine several of these techniques together to achieve higher levels of performance and adaptability The discussion also includes how to employ

specialized software to improve this new adaptive system and how this new kind of software must be designed and programmed **Autonomic Networking-on-Chip** Phan Cong-Vinh,2018-09-03 Despite the growing mainstream importance and unique advantages of autonomic networking on chip ANoC technology Autonomic Networking On Chip Bio Inspired Specification Development and Verification is among the first books to evaluate research results on formalizing this emerging NoC paradigm which was inspired by the human nervous system The FIRST Book to Assess Research Results Opportunities Trends in BioChipNets The third book in the Embedded Multi Core Systems series from CRC Press this is an advanced technical guide and reference composed of contributions from prominent researchers in industry and academia around the world A response to the critical need for a global information exchange and dialogue it is written for engineers scientists practitioners and other researchers who have a basic understanding of NoC and are now ready to learn how to specify develop and verify ANoC using rigorous approaches Offers Expert Insights Into Technical Topics Including Bio inspired NoC How to map applications onto ANoC ANoC for FPGAs and structured ASICs Methods to apply formal methods in ANoC development Ways to formalize languages that enable ANoC Methods to validate and verify techniques for ANoC Use of self processes in ANoC self organization configuration healing optimization protection etc Use of calculi for reasoning about context awareness and programming models in ANoC With illustrative figures to simplify contents and enhance understanding this resource contains original peer reviewed chapters reporting on new developments and opportunities emerging trends and open research problems of interest to both the autonomic computing and network on chip communities Coverage includes state of the art ANoC architectures protocols technologies and applications This volume thoroughly explores the theory behind ANoC to illustrate strategies that enable readers to use formal ANoC methods yet still make sound judgments and allow for reasonable justifications in practice Proceedings of the FISITA 2012 World Automotive Congress SAE-China,FISITA,2012-10-26 Proceedings of the FISITA 2012 World Automotive Congress are selected from nearly 2 000 papers submitted to the 34th FISITA World Automotive Congress which is held by Society of Automotive Engineers of China SAE China and the International Federation of Automotive Engineering Societies FISITA This proceedings focus on solutions for sustainable mobility in all areas of passenger car truck and bus transportation Volume 6 Vehicle Electronics focuses on Engine Chassis Body Electronic Control Electrical and Electronic System Software and Hardware Development Electromagnetic Compatibility EMC Vehicle Sensor and Actuator In Vehicle Network Multi Media Infotainment System Above all researchers professional engineers and graduates in fields of automotive engineering mechanical engineering and electronic engineering will benefit from this book SAE China is a national academic organization composed of enterprises and professionals who focus on research design and education in the fields of automotive and related industries FISITA is the umbrella organization for the national automotive societies in 37 countries around the world It was founded in Paris in 1948 with the purpose of bringing engineers from around the world together in a spirit of

cooperation to share ideas and advance the technological development of the automobile   Proceedings ,1996

Hardware Supply Chain Security Basel Halak,2021-02-04 This book presents a new threat modelling approach that specifically targets the hardware supply chain covering security risks throughout the lifecycle of an electronic system The authors present a case study on a new type of security attack which combines two forms of attack mechanisms from two different stages of the IC supply chain More specifically this attack targets the newly developed light cipher Ascon and demonstrates how it can be broken easily when its implementation is compromised with a hardware Trojan This book also discusses emerging countermeasures including anti counterfeit design techniques for resources constrained devices and anomaly detection methods for embedded systems   *Cognitive Networks* Qusay Mahmoud,2007-09-11 Cognitive networks can dynamically adapt their operational parameters in response to user needs or changing environmental conditions They can learn from these adaptations and exploit knowledge to make future decisions Cognitive networks are the future and they are needed simply because they enable users to focus on things other than configuring and managing networks Without cognitive networks the pervasive computing vision calls for every consumer to be a network technician The applications of cognitive networks enable the vision of pervasive computing seamless mobility ad hoc networks and dynamic spectrum allocation among others In detail the authors describe the main features of cognitive networks clearly indicating that cognitive network design can be applied to any type of network being fixed or wireless They explain why cognitive networks promise better protection against security attacks and network intruders and how such networks will benefit the service operator as well as the consumer Cognitive Networks Explores the state of the art in cognitive networks compiling a roadmap to future research Covers the topic of cognitive radio including semantic aspects Presents hot topics such as biologically inspired networking autonomic networking and adaptive networking Introduces the applications of machine learning and distributed reasoning to cognitive networks Addresses cross layer design and optimization Discusses security and intrusion detection in cognitive networks Cognitive Networks is essential reading for advanced students researchers as well as practitioners interested in cognitive wireless networks pervasive computing distributed learning seamless mobility and self governed networks With forewords by Joseph Mitola III as well as Sudhir Dixit   *Tradeoffs and Optimization in Analog CMOS Design* David Binkley,2008-09-15 Analog CMOS integrated circuits are in widespread use for communications entertainment multimedia biomedical and many other applications that interface with the physical world Although analog CMOS design is greatly complicated by the design choices of drain current channel width and channel length present for every MOS device in a circuit these design choices afford significant opportunities for optimizing circuit performance This book addresses tradeoffs and optimization of device and circuit performance for selections of the drain current inversion coefficient and channel length where channel width is implicitly considered The inversion coefficient is used as a technology independent measure of MOS inversion that permits design freely in weak moderate and strong inversion This book details

the significant performance tradeoffs available in analog CMOS design and guides the designer towards optimum design by describing An interpretation of MOS modeling for the analog designer motivated by the EKV MOS model using tabulated hand expressions and figures that give performance and tradeoffs for the design choices of drain current inversion coefficient and channel length performance includes effective gate source bias and drain source saturation voltages transconductance efficiency transconductance distortion normalized drain source conductance capacitances gain and bandwidth measures thermal and flicker noise mismatch and gate and drain leakage current Measured data that validates the inclusion of important small geometry effects like velocity saturation vertical field mobility reduction drain induced barrier lowering and inversion level increases in gate referred flicker noise voltage In depth treatment of moderate inversion which offers low bias compliance voltages high transconductance efficiency and good immunity to velocity saturation effects for circuits designed in modern low voltage processes Fabricated design examples that include operational transconductance amplifiers optimized for various tradeoffs in DC and AC performance and micropower low noise preamplifiers optimized for minimum thermal and flicker noise A design spreadsheet available at the book web site that facilitates rapid optimum design of MOS devices and circuits Tradeoffs and Optimization in Analog CMOS Design is the first book dedicated to this important topic It will help practicing analog circuit designers and advanced students of electrical engineering build design intuition rapidly optimize circuit performance during initial design and minimize trial and error circuit simulations **Principles of Asynchronous Circuit Design** Jens Sparsø,Stephen Bo Furber,2001-12-31 Principles of Asynchronous Circuit Design A Systems Perspective addresses the need for an introductory text on asynchronous circuit design Part I is an 8 chapter tutorial which addresses the most important issues for the beginner including how to think about asynchronous systems Part II is a 4 chapter introduction to Balsa a freely available synthesis system for asynchronous circuits which will enable the reader to get hands on experience of designing high level asynchronous systems Part III offers a number of examples of state of the art asynchronous systems to illustrate what can be built using asynchronous techniques The examples range from a complete commercial smart card chip to complex microprocessors The objective in writing this book has been to enable industrial designers with a background in conventional clocked design to be able to understand asynchronous design sufficiently to assess what it has to offer and whether it might be advantageous in their next design task Hardware Security: Challenges and Solutions Ashutosh Mishra,Mrinal Goswami,Manoj Kumar,Navin Singh Rajput,2025-03-03 This book provides a comprehensive overview of hardware security challenges and solutions making it an essential resource for engineers researchers and students in the field The authors cover a wide range of topics from hardware design and implementation to attack models and countermeasures They delve into the latest research and industry practices in the field including techniques for secure chip design hardware Trojan detection side channel attack mitigation the threats and vulnerabilities facing modern hardware the design and implementation of secure hardware and the latest techniques for testing and verifying the security of hardware

systems The book also covers emerging technologies such as quantum computing and the Internet of Things and their impact on hardware security With its practical approach and extensive coverage of the subject this book is an ideal reference for anyone working in the hardware security industry **System-on-Chip for Real-Time Applications** Wael Badawy,Graham A. Julien,2012-12-06 System on Chip for Real Time Applications will be of interest to engineers both in industry and academia working in the area of SoC VLSI design and application It will also be useful to graduate and undergraduate students in electrical and computer engineering and computer science A selected set of papers from the 2nd International Workshop on Real Time Applications were used to form the basis of this book It is organized into the following chapters Introduction Design Reuse Modeling Architecture Design Techniques Memory Circuits Low Power Interconnect and Technology MEMS System on Chip for Real Time Applications contains many signal processing applications and will be of particular interest to those working in that community *Low Power Networks-on-Chip* Cristina Silvano,Marcello Lajolo,Gianluca Palermo,2010-09-24 In recent years both Networks on Chip as an architectural solution for high speed interconnect and power consumption as a key design constraint have continued to gain interest in the design and research communities This book offers a single source reference to some of the most important design techniques proposed in the context of low power design for networks on chip architectures **Optimal Synthesis Methods for MEMS** S.G.K. Ananthasuresh,2012-12-06 The field of microelectromechanical systems or MEMS has gradually evolved from a discipline populated by a small group of researchers to an enabling technology supporting a variety of products in such diverse areas as mechanical and inertial sensors optical projection displays telecommunications equipment and biology and medicine Critical to the success of these products is the ability to design them and this invariably involves detailed modeling of proposed designs Over the past twenty years such modeling has become increasingly sophisticated with full suites of MEMS oriented computer aided design tools now available worldwide But there is another equally important side to the design process In my own book Microsystem figuring out what to build in the first place Design I chose to emphasize the modeling aspect of design The task of figuring out what to build was defined by a vague step called creative thinking I used practical product examples to illustrate the many subtle characteristics of successful designs but I made no attempt to systematize the generation ofdesign proposals or optimized designs That systemization is called synthesis which is the subjectofthis book Integrated Circuits for Analog Signal Processing Esteban Tlelo-Cuautle,2012-07-27 This book presents theory design methods and novel applications for integrated circuits for analog signal processing The discussion covers a wide variety of active devices active elements and amplifiers working in voltage mode current mode and mixed mode This includes voltage operational amplifiers current operational amplifiers operational transconductance amplifiers operational transresistance amplifiers current conveyors current differencing transconductance amplifiers etc Design methods and challenges posed by nanometer technology are discussed and applications described including signal amplification filtering data acquisition systems such as neural

recording sensor conditioning such as biomedical implants actuator conditioning noise generators oscillators mixers etc Presents analysis and synthesis methods to generate all circuit topologies from which the designer can select the best one for the desired application Includes design guidelines for active devices elements with low voltage and low power constraints Offers guidelines for selecting the right active devices elements in the design of linear and nonlinear circuits Discusses optimization of the active devices elements for process and manufacturing issues of nanometer technology

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