

A Direct Digital Frequency Synthesis System for Low Power Communications

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Abstract

This work describes a Direct Digital Frequency Synthesis (DDFS) architecture based on nonlinear interpolation for signal generation in mobile communications systems such as Bluetooth. DDFS is capable of well controlled, rapid changes in frequency, over a relatively large frequency range, however a conventional DDFS system requires a power hungry ROM. To avoid this problem a ROM-less architecture with a low power nonlinear interpolation DAC is proposed. This system is robust to parameter variations and consumes only 5mW at 100MHz.

1. Introduction

A conventional DDFS system consists of an L-bit accumulator which occasionally overflows, providing a periodic sequence of numbers which represents phase of the output waveform. This phase is used to address a lookup table of amplitude values stored in a ROM and passed through a corresponding DAC to create a synthesised, analogue signal (Figure 1.). The ROM consumes most of the power of the system and several alternative architectures for ROM reduction have therefore been investigated [1, 2, 3].

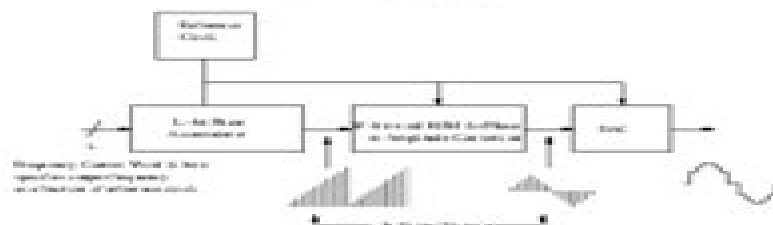


Figure 1. DDFS system architecture.

Quantisation caused by ROM size reduction and non-idealities associated with the DAC cause the generation of spectral power at unwanted frequencies, corrupting the DDFS output. This effect is measured as

SFDR, which is the difference in power between the synthesised signal and the next most powerful (unwanted) frequency in the output spectrum. The SFDR requirement of a Bluetooth system is -50 dBc [4]. The Bluetooth specification also requires a channel bandwidth of 1MHz which is frequency hopped over 79 channels every 625 μ s, with frequency resolution of 1ppm.

Dynamic performance of DDFS systems rapidly degrades with frequency due to transient glitches in the DAC. These glitches can be minimised by using a current switched cell (Figure 2.) and thermometer decoding to reduce dynamic errors by ensuring that the minimum number of cells switch simultaneously. Additionally the use of latches for all switching signals ensures that all cells switch synchronously and the use of differential switches allows reduction of the voltage required to switch the current cell. However timing skew cannot be completely removed and state of the art low power RF CMOS DACs are limited to approximately -70 dBc SFDR [5, 6].

The interpolation method is introduced in section 2 with Matlab projections of system performance. Section 3 presents the architecture of a prototype system and section 4 demonstrates that the system is robust to process variations. Results and power consumption are shown in Section 5.

2. Nonlinear DAC interpolation method

The ROM may be replaced by using a nonlinear DAC to perform both phase to amplitude conversion as well as digital to analogue conversion. A nonlinear weighted array of current cells is used to store the phase to amplitude information within the DAC. Using a trigonometric approximation, Kang and Lee [2] designed a ROM-less DDFS system consisting of 192 current cells. This system has an SFDR of better than -60 dBc at low synthesised frequencies (less than 10 MHz), which degrades to worse than -55dBc at higher frequencies (up to 100 MHz). To reduce the number of current cells a technique is proposed which employs each current cell more efficiently.

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1. Understanding the eBook Arrls Low Power Communications
 - The Rise of Digital Reading Arrls Low Power Communications
 - Advantages of eBooks Over Traditional Books
2. Identifying Arrls Low Power Communications
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Arrls Low Power Communications
 - User-Friendly Interface
4. Exploring eBook Recommendations from Arrls Low Power Communications
 - Personalized Recommendations
 - Arrls Low Power Communications User Reviews and Ratings
 - Arrls Low Power Communications and Bestseller Lists
5. Accessing Arrls Low Power Communications Free and Paid eBooks
 - Arrls Low Power Communications Public Domain eBooks
 - Arrls Low Power Communications eBook Subscription Services
 - Arrls Low Power Communications Budget-Friendly Options
6. Navigating Arrls Low Power Communications eBook Formats

- ePub, PDF, MOBI, and More
- Arrls Low Power Communications Compatibility with Devices
- Arrls Low Power Communications Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Arrls Low Power Communications
 - Highlighting and Note-Taking Arrls Low Power Communications
 - Interactive Elements Arrls Low Power Communications
- 8. Staying Engaged with Arrls Low Power Communications
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Arrls Low Power Communications
- 9. Balancing eBooks and Physical Books Arrls Low Power Communications
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Arrls Low Power Communications
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Arrls Low Power Communications
 - Setting Reading Goals Arrls Low Power Communications
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Arrls Low Power Communications
 - Fact-Checking eBook Content of Arrls Low Power Communications
 - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
- 14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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